WHAT IS CLAIMED IS:

1. A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied; and

a logic circuit to which a second pulse signal outputted from said clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein

said clocked inverter circuit changes a pulse width of said first pulse signal in a direction opposite to a direction in which a pulse width of a third pulse signal outputted from said logic circuit changes.

2. The delay circuit according to claim 1, wherein said logic circuit is a NOR circuit and said clocked inverter circuit delays a trailing edge of said third pulse signal.

3. The delay circuit according to claim 1, wherein said logic circuit is a NAND circuit and said clocked inverter circuit delays a leading edge of said third pulse signal.

4. The delay circuit according to claim 1, wherein said clocked inverter circuit is composed of an NMOS transistor and a PMOS transistor and at least one of a channel width, channel length, threshold voltage, and substrate voltage of the NMOS is different from a channel width, channel length, threshold voltage, and substrate voltage of the PMOS transistors.

5. The delay circuit according to claim 4, wherein a ratio of a current driving capability of said PMOS transistor to a current driving capability of said NMOS transistor is set to a value other than one and a rise time of a pulse signal is made different from a decay time of the pulse signal.

6. A delay circuit comprising:

an inverter circuit controlled by a clock signal to which a first pulse signal is supplied; and

a logic circuit to which a second pulse signal outputted from said inverter circuit and an inverted signal of said first pulse signal are supplied, wherein

said inverter circuit changes a pulse width of said first pulse signal in a direction opposite to a direction in which a pulse width of a third pulse signal outputted from said logic circuit changes.

Add a4

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